10.5 A 10b 10GHz Digitally Controlled LC Oscillator in 65nm CMOS

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A digitally controlled LC oscillator (DCO) is integrated in a digital 65nm CMOS technology. The frequency of the DCO can be fine tuned with 10 control bits from 9.87GHz to 10.92GHz (10%) with an average frequency step of 1.03MHz/LSB. The DCO consumes 3.0mA from a 1.1V supply and achieves a phase noise of -102dBc/Hz at 1MHz offset (FOM=-177.2dBc/Hz). The minimum size transistors offered by the 65nm technology are exploited to shrink the area of the varactor bank in 70×70μm² and to reduce the tank parasitic capacitance.

The scaling of CMOS technology and supply voltages and the integration of analog front-ends into noisy digital SoCs have recently pushed the implementation of PLLs in a digital manner as a promising alternative to the analog one [1, 2, 3]. A key component for high-performance fully integrated digital PLLs is the availability of low-noise digitally controlled oscillators [4].

An LC oscillator has been implemented whose frequency is controlled by a 10b frequency control word. The block diagram of the DCO is shown in Fig. 10.5.1. The DCO consists of a PMOS bias current source, cross-coupled PMOS and NMOS transistors to provide the gain, a 0.84nH integrated inductor, and an array of PMOS varactor cells connected in parallel to the inductor and providing the tuning. For testing purposes the DCO output is ac coupled to a CML divide-by-8 circuit and driven off chip.

Low power consumption and high tuning range require a low fixed parasitic capacitance of the LC tank. This is difficult to achieve in high-resolution DCOs. Here, special measures have been taken both at the architecture level as well as layout level, which will be explained hereafter. It is not feasible to control each varactor individually, since 10b resolution would mean to layout 1024 control lines into the array leading to severe routing problems, waste of area, and higher parasitics. The number of lines to route can be drastically reduced by arranging the varactor array into a matrix of cells, each including a varactor and a local decoder to decode the input frequency control word.

This arrangement would require a matrix of 32×32 cells. For fine frequency resolution the size of the PMOS varactor is close to the minimum allowed by the technology, so that the cell area would be dominated by the local decoder. To save area and reduce parasitics, the size of the matrix can be shrunk by creating two cells types: a first one (type1) with a local decoder controlling 4 PMOS in parallel (see Fig. 10.5.2) and a second one (type2) where the decoder controls only one PMOS varactor.

This leads to the final implementation shown in Fig. 10.5.1. Bits *fcw[9:6]* and *fcw[5:2]* are thermometer decoded and latched to eliminate glitches due to different propagation times of the converters. The outputs of the latches deliver the column information *c[15:0]* and *w[15:0]* and the row information *r[15:0]* to a 16×16 matrix of type1 cells. In this way, only 48 lines need to be routed through the matrix and its area is reduced to 25% as compared to that of a 32×32 cells matrix. Bits *fcw[1:0]* are also thermometer decoded into *s[2:0]* and control three type2 cells.

For low-jitter digital PLLs, the DCO frequency step corresponding to 1LSB must be as constant as possible along the whole tuning range (small DNL), requiring excellent layout matching between type1 and type2 cells. The matching is improved by: first, laying out the type2 cells almost identically to the type1 cells, with the only difference that just 1 out of the 4 PMOS varactors is connected to the local decoder. Secondly, the type2 cells are physically placed as equally distributed as possible inside the 16×16 matrix (see Fig. 10.5.1).

A critical point for DNL is the switching from the last cell of one row to the first of the next row. Our experience shows that it is not enough to turn on the cells of the array in a meander way. It is also important that not too many control lines (*c, w,* or *r*) change their status (digital high or low) at the same time. This is achieved by designing different local decoders in the even and odd columns (see Fig. 10.5.2). While the capacitance in an odd column is turned on if *w AND (c OR r)*, the logic of the decoder in an even column is inverted and the capacitance is turned on if *w NOR (c AND r)*. Moreover, the *r* of the first cell in each column is stuck to one (odd column) or zero (even column). In this way the matrix can be turned on in a meander way and the switch from one column to the next one requires changing the status of only one *c* and one *w* control line. The local decoders use minimum length transistors (W=180nm L=60nm) while for the varactors W=90nm and L=120nm to reduce the gate overlap capacitances. For better matching between even and odd columns, transistors M1 to M8 are laid out identically. Only the connections to the control lines are different. That's why, for instance, transistors M5 and M6 in the odd columns are connected in series.

Figure 10.5.3 shows the phase noise measured after the divide-by-8 block and recalculated to the 10.5GHz carrier. This measurement contains also the noise produced by the CML divider. The flicker noise corner is 400kHz due to the minimum L=60nm dimension of the cross coupled transistors in the oscillator. The FOM is calculated according to [5]:

$$FOM = S_{SSB}(\Delta f) \cdot \left(\frac{\Delta f}{f_0}\right)^2 P_{VCO} / mW$$

and is equal to -177.2dBc/Hz.

The measured tuning curve of the DCO is shown in Fig. 10.5.4 top left. The output frequency goes from 9.87 to 10.92GHz quite linearly. The DNL (Fig. 10.5.4, bottom) is ≤0.52LSB and is dominated by the mismatch between the type1 and type2 cells in the matrix. Indeed, only every fourth point in the DNL deviates substantially from the mean value (see Fig. 10.5.4, top right). Since the inductor has a value of 0.84nH, the tank capacitance amounts to 270fF. The average frequency step is 1.03MHz/LSB, corresponding to a switched capacitance of 55aF/LSB.

Figure 10.5.5 is a measurement of the sensitivity of the DCO frequency to supply variations measured from 1.0V to 1.2V. Figure 10.5.6 summarizes the performances and Fig. 10.5.7 is a layout plot. The varactor matrix including the two thermometer decoders can clearly be seen below the inductor. The complete DCO occupies an area of 112×220μm².

References:

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[2] J. Lin et al, "A PVT Tolerant 0.18MHz to 600MHz Self-Calibrated Digital PLL in 90nm CMOS Process," *ISSCC Dig. Tech. Papers*, pp. 488-489, Feb., 2004.

[3] N. Da Dalt et al, "A Compact Triple-Band Low-Jitter Digital LC PLL With Programmable Coil in 130-nm CMOS," *IEEE J. Solid-State Circuits*, Vol. 40, No. 7, pp.1482-1490, July, 2005,

[4] R. Staszewski et al. "A First Multigigahertz Digitally Controlled Oscillator for Wireless Applications," *IEEE Trans. MTT*, vol. 51, no. 11, pp. 2154-2164, Nov., 2003.

[5] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum" Proc. IEEE, pp. 329–330, Feb., 1966.

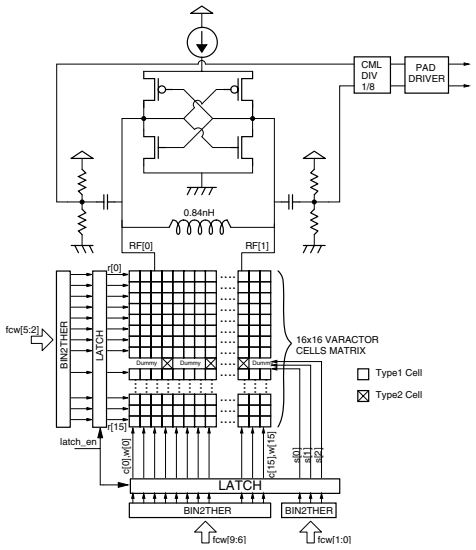

Figure 10.5.1: DCO block diagram.

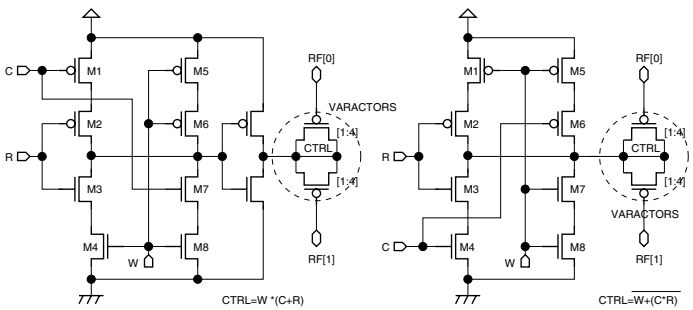

Figure 10.5.2: Schematic of type1 varactor cell for odd columns (left) and even columns (right).

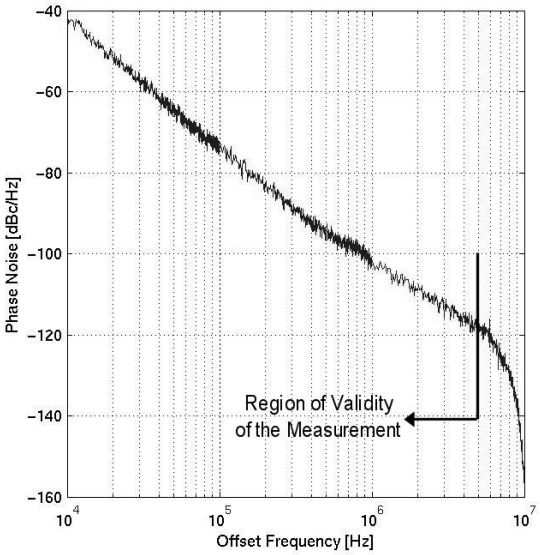

Figure 10.5.3: Measured DCO phase noise at 10.5GHz.

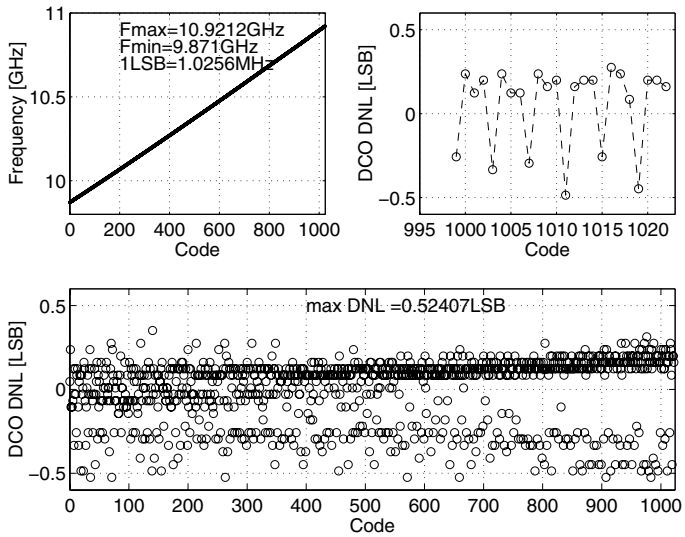

Figure 10.5.4: Measured DCO output tuning range and DNL.

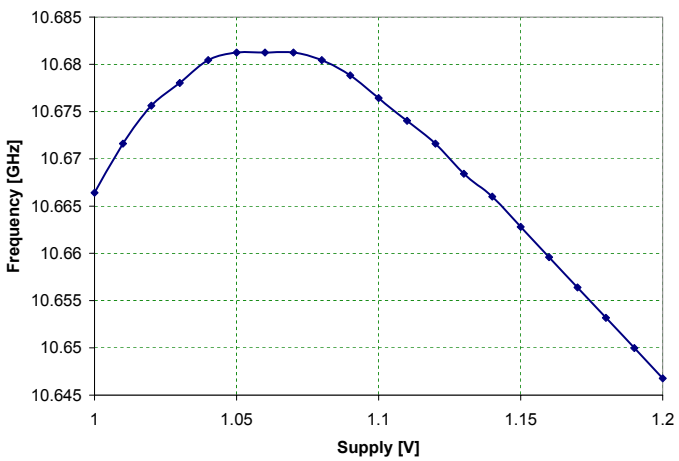

Figure 10.5.5: Measured DCO frequency sensitivity to supply variations (dc).

Frequency Range	9.87GHz to 10.92GHz
Tuning range	10%
DCO Gain	1.03MHz/LSB
DCO DNL	0.52 LSB
Phase Noise	-102 dBc/Hz @ 1MHz
Supply Pulling	<50MHz/100mV (DC, at 1.0V)
Power supply	1.1V
Current consumption DCO CML divider by 8 Offchip Driver	 3.0 mA 6.1 mA 24 mA
DCO area	112μm x 220μm
Technology	Digital 65nm CMOS, 6ML
FOM	-177.2 dBc/Hz

Figure 10.5.6: Performance summary.

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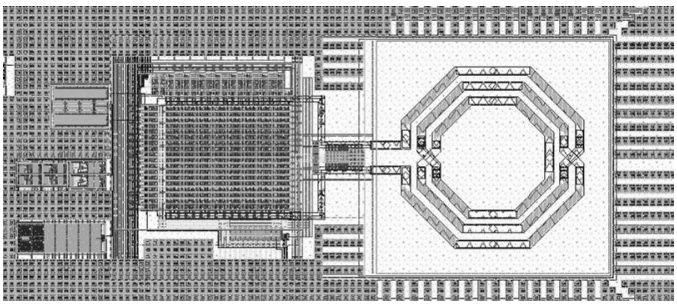

Figure 10.5.7: DCO layout.

